

Application No.: 09/671,567

Docket No.: JCLA5635

**Remarks**

It is noted with great appreciation that claims 1-9 are allowed. The Office Action rejected claims 10-12 as being unpatentable over Younse et al. (USP 4,805,203) in view of Ayukawa et al. (USP 6,404,694) and further in view of Heller et al. (USP 6,396,539).

After carefully considering the remarks set forth in this Office Action and the cited references, Applicants respectfully traverse the rejection and submit the following remarks. Reconsideration and withdrawal of the rejection is requested.

**Discussion of 35 U.S.C §103 rejections**

*Claims 10 and 12 are rejected under 35 U.S.C 103(a) as being unpatentable over Younse et al. (USP 4,805,023, Younse hereinafter) in view of Ayukawa et al. (USP 6,404,694, Ayukawa hereinafter).*

Claim 10 recites "a memory element for storing a plurality of defective pixel addresses, wherein the defective pixel addresses are arranged in an ascending order in the memory element". Having the defective pixel addresses arranged in an ascending order, the index can be simply increased by one unit for commencing another address comparison cycle when there is a hit. Absent such an ordered arrangement for the defective pixel addresses, the comparison cycle time will increase because each defective pixel address may have to be compared again. Applicants respectfully disagree with the Office's assertion that there is no distinction between the addresses of the data items being consecutive and the data items being consecutive. In the embodiment of the present invention, the data items, which are the defective pixel addresses, are arranged in an ascending order. When the sensor address and the defective address are the same, the address

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comparator will output a flag indicating the current pixel of the image sensor is defective and the index (or the address) for the data items is increased by one (for example, from index=0 to index=1) to begin another address comparison cycle. In other words, for the next sensor address, comparison will commence with the data items in index=1. On the other hand, if only the addresses of the data items are consecutive (not the actual data items) as in Ayukawa, and the data items stored in the consecutive addresses are not in consecutive order, each comparison cycle may have to start with index=0. For example, if the data item in index=0 is 0010 and the data item in index=1 is 0001 and the first sensor address is 0001, to compare the second sensor address, the comparison cycle may have to start with index=0 again.

Therefore, with the fact that Ayukawa teaches that the addresses of the data items are consecutive, not the actual data items, the combination of Younse and Ayukawa still fails to render claim 10 of the present invention unpatentable. Applicants therefore respectfully request the withdrawal of the rejection under 35 U.S.C. §103(a) of claims 10 & 12.

*Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Younse et al. in view of Heller et al. (U.S. Patent 6,396,539).*

For at least the reasons that Heller also fails to disclose the defective pixel addresses are arranged in an ascending order in the memory element. Even Heller teaches the memory element is a fuse array, the combination of Heller with Younse still fails to remedy the deficiency in Younse. Accordingly, Applicants respectfully assert that Younse in view of Heller fails to render claims 11 obvious. Thus, reconsideration and withdrawal of this rejection are respectively requested.

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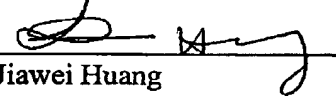
**CONCLUSION**

For at least the reasons set forth above, Applicants respectfully submit that the rejections should be withdrawn, and that all pending claims 1-12 are in conditions for allowance. If, in the opinion of the Examiner, a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

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Respectfully submitted,  
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